Amendments to the Specification:

Please replace the paragraph beginning at line 16, page 2, with the following rewritten paragraph:

Firewall 110 includes a public network link 120, private network link 122 and memory controller 124 coupled by a bus (e.g., PCI bus) 125. Memory controller 124 is coupled to a memory (RAM) 126 and firewall engine 128 by a memory bus 129. Firewall engine 128 performs packet screening prior to routing packets through to private network 102. A central processor (CPU) [[132]] 134 is coupled to memory controller 124 by a CPU bus [[134]] 132. CPU [[132]] 134 oversees the memory transfer operations on all buses shown. Memory controller 124 is a bridge connecting CPU Bus [[134]] 132, memory bus 129 and PCI bus 125.

Please replace the paragraph beginning at line 27, page 6, with the following rewritten paragraph:

A central processor (CPU) [[132]] 134 is coupled to memory controller 124 by CPU bus [[134]] 132. CPU [[132]] 134 oversees the memory transfer operations on memory bus 129 and bus 125.

Please replace the paragraph beginning at line 30, page 6, with the following rewritten paragraph:

Referring now to FIGS. 2 and 3, a process 300 for screening packets is described in general. Packets are received at public network link 120 (302). Each packet is transferred on bus 125 to, and routed through, memory controller 124 and on to dual-port

memory (RAM) 203 via memory bus 129 (304). When ASIC 204 is available, the packet is fetched by ASIC 204 using local bus 202 (306). After processing by ASIC 204 (308), the packet is returned to RAM [[126]] 203 using local bus 202 (310). The processing by ASIC 204 can include authentication, encryption, decryption, virtual private network (VPN) and firewall services. Finally, the packet is retrieved by memory controller 124 using memory bus 129 (312), and routed to private network link 122 (314).